REMARKS

Claims 1 – 32 were pending in the Application prior to the outstanding Office Action, with claims 19 – 31 having been withdrawn as applying to a non-elected species. In the Listing of Claims, Applicant has amended Claims 1, 5 – 7, 9, 11, 13, 15, 17, 19, 21 – 24, 26, 28, 30 and 32.

The Examiner is thanked for the telephone conference held on July 11, 2007 and the opportunity to discuss the present application.

In the Office Action, the Examiner rejected Claim 32 under 35 U.S.C. §112, second paragraph as indefinite. This rejection is discussed below.

I. RESPONSE TO REJECITONS UNDER 35 U.S.C. §112, SECOND PARAGRAPH

In the Office Action, the Examiner expresses confusion over the language of Claim 32, which previously recited a "direct transition" between a first state and a second state and had further stated that such a direct transition is both "generated" in one circumstance and "prevented" in another circumstance. Specifically the Examiner asks: "is this the same 'direct transition' that the logic circuit generates or is this a different 'direct transition?' ... if this is the same 'direct transition' how is it prevented after it has occurred in relation to the logic circuit?" The Examiner also asks: "if the host prevents a 'direct transition' what or how is the host generating another 'direct transition' in the last passage of the claim?"

In answer to these questions, the Applicant points out that Claim 32 as previously composed recited a "direct transition" to refer to a type of event that arises when signals change, rather than a specific event. As such, this event or condition is generated in one circumstance and is prevented in another circumstance. Specifically, the condition of a direct transition is purposefully created to perform input from or output to an expansion circuit and is purposefully avoided to perform input from or output to a peripheral device. In a preferred embodiment, the invention allows an expansion circuit to co-exist with a peripheral device, so that both types of access can occur.

Specifically, by "direct transition," Applicant means the condition that occurs when a plurality of signals change from one state to another state without going through a third state. For example, in the embodiment illustrated in Figure 4B, the transition labeled "D" represents a direct transition between the 00 state and the 10 state. Figure 4A also illustrates this transition with the dotted line labeled "D," where signal D0 stays low and signal D1 changes from low to high. The dotted line labeled "B" in Figures 5A and 6A and the transition labeled "B" in Figures 5B and 6B are other examples of a direct transition between the 00 state and the 10 state.

In contrast, the circumstance illustrated in Figure 3B has no direct transitions between the 00 state and the 10 state. Instead, the signals D0 and D1 transition through a third state, for example through the 01 state and/or the 11 state. In particular, in Figures 3A and 3B, in order to transition between the 00 state and the 10 state, the signals go through the sequence 00 → 01 → 11 → 10. Claim 32 as amended recites that "said first and second signals transition to a third state after said first state and before said second state when the state of said first and second signals are changed as necessary to perform input from or output to said peripheral device." Figures 3A and 3B illustrate an embodiment of performing input from or output to a peripheral device.

Claim 32 as amended also recites the generation of an internal signal in response to "the condition wherein said first and second signals transition directly between a first state and a second state." In the embodiments illustrated in Figures 4A, 5A and 6A, the internal signal is labeled "Internal Enable/Strobe" and "Internal Strobe." As illustrated in these figures, this signal is generated in response to the direct transition between the 00 state and the 10 state as explained above. Claim 32 as amended further recites that "said first and second signals transition directly between said first state and said second state when the state of said first and second signals are changed as necessary to perform input from or output to said expansion circuit." Figures 4A, 4B, 5A, 5B, 6A and 6B illustrate embodiments of performing input from or output to an expansion circuit.

In the Office Action, the Examiner also states: "Examiner is unsure of the clocking of the first and second state, in other words, is the 'direct transition' in one clocking cycle or a first clock cycle for the first state and a second clock cycle for the second state?" In answer to this question, Applicant points out that the circuitry of the preferred embodiment operates asynchronously, without the need for a clock signal and without the need for clock cycles. For example, as illustrated in Figures 4A and 4B, the transition labeled "D" represents the condition where the D0 signal stays at a logic low level while the signal D1 transitions from a logic low level to a logic high level. The occurrence of this transition itself, separate from any clocking, is the condition that causes the internal signal labeled "Internal Strobe/Enable" to be generated. Paragraph 0023 of the specification also explains that in one embodiment the expansion circuit is coupled only to data lines and not to any control lines (such as clock signals). The circuits illustrated in Figures 7 and 8 operate by monitoring of the instantaneous values of the states of the data signals (i.e. the logic levels of the D0 and D1 lines) and thus do not need any clock signal inputs from the host controller.

ADDITIONAL REMARKS

Applicant notes claim 32 is a generic claim and upon which all the claims of Species 1 (claims 1 – 18) and all of the claims of Species 2 (claims 19 – 31) depend, directly or indirectly. Accordingly, if claim 32 is allowed, applicants request rejoinder of the Species 2 claims as provided for in MPEP 821.04.

Respectfully submitted,

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